AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for placing circuit elements on an integrated circuit, the method comprising:

a) placing cells of a ~~first~~ circuit design by use of non-direct timing driven processes~~, wherein said placing produces a first placement~~; ~~and~~

b) providing routing information associated with said cells;

c) performing an incremental placement of said cells using said routing information;

~~b~~ d) placing said cells by use of direct timing driven placement processes~~, wherein said first placement is an input into said b) placing~~; and

e) repeating b) and c) after d) to optimize placement of said cells.

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2. (Currently Amended) The method of Claim 1 wherein ~~said a~~ b) comprises:

~~a1) placing cells of said first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said a1) placing produces said first placement~~

estimating routability of said cells; and

enlargening areas associated with said cells, as necessary, based on said routability.

3. (Currently Amended) A method for placing circuit elements on an integrated circuit, the method comprising:

a) placing cells of a ~~first~~ circuit design by use of non-direct timing driven processes~~, wherein said a) placing produces a first placement~~;

b) routing wiring to connect said cells, ~~wherein said routing produces~~ thereby generating a ~~first~~ layout;

c) ~~modifying said first circuit design to produce second cells of a second circuit design~~ minimizing required signal timing within said layout; ~~and~~

d) performing an incremental placement of said cells;

e) placing said ~~second~~ cells by use of direct timing driven placement processes; and

f) repeating b), c), and d) after e) to optimize placement of said cells.

4. (Currently Amended) The method of Claim 3 wherein ~~said~~ a) comprises:

B1 a1) placing cells ~~of said first circuit design~~ to minimize total weighted length of wiring interconnecting said cells~~,~~ ~~wherein said a1) placing produces said first placement~~.

5. (Currently Amended) The method of Claim 3 wherein ~~said~~ b) comprises:

b1) estimating congestion for wiring to connect said cells~~,~~ ~~wherein said first placement is said first layout~~.

6. (Currently Amended) The method of Claim 3 wherein ~~said~~ c) ~~comprises:~~ includes at least one of:

~~c1) modifying said first circuit design to achieve minimum required signal timing within said first layout, wherein said modifying produces said second circuit design containing second cells~~ changing a current-handling capacity of a circuit element and adding a buffer.

7. (Currently Amended) The method of Claim 3 wherein ~~said~~ c) comprises:

c1) modifying said ~~first~~ circuit design to enlarge cell area allocations within congested regions of said ~~first~~ layout~~, wherein said modifying produces said second circuit design containing second cells~~.

8. (Currently Amended) A method for placing circuit elements on an integrated circuit, the method comprising:

a) placing cells of a ~~first~~ circuit design by use of non-direct timing driven processes~~, wherein said placing produces a first placement~~;

b) routing ~~said~~ wiring to connect said cells, ~~wherein said routing produces~~ thereby generating a ~~first~~ layout;

B1 c) synthesizing said layout to optimize timing;

d) performing an incremental placement of said cells based on said synthesizing;

~~e~~ e) placing said cells by use of direct timing driven placement processes ~~to produce a new placement, wherein said first layout is an input into said e) placing~~;

~~d) routing said new placement, wherein said d) routing produces a new layout;~~ and

~~e~~ f) ~~placing said cells by use of direct timing driven placement processes to produce another new placement, wherein said new layout is an input into said e) placing~~ repeating b), c), and d) after e) to optimize placement of said cells.

9. (Currently Amended) The method of Claim 8 wherein ~~said~~ a) comprises:

a1) ~~placing cells of said first circuit design to minimize~~ minimizing total weighted length of wiring interconnecting said cells~~, wherein said ai) placing produces said first placement~~.

10. (Currently Amended) The method of Claim 8 wherein ~~said~~ b) comprises:

b1) estimating congestion for wiring to connect said cells~~, wherein first placement is further a first layout~~.

11. (Currently Amended) The method of Claim 8 ~~further comprising repeating said d) and e)~~ wherein c) comprises:

c1) at least one of modifying a cell and adding another cell to meet timing constraints.

12. (Currently Amended) A method for placing circuit elements on an integrated circuit, the method comprising:

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a) synthesizing a high level description of a circuit to produce a ~~first~~ circuit design;

b) placing cells of said ~~first~~ circuit design by use of one of b1) non-direct timing driven processes~~, wherein said placing produces a first placement~~ and b2) direct timing driven processes;

c) routing wiring to connect said cells, ~~wherein said routing produces~~ thereby generating a ~~first~~ layout;

d) modifying ~~said first circuit design to produce~~ cell area allocations in said layout, if necessary to relieve congestion ~~a second high level description of a circuit~~;

e) ~~synthesizing said second high level description of a circuit to produce a second circuit design~~ performing a post-layout synthesis optimization with said cells; and

f) providing an incremental placement of said cells,

~~f) placing second cells of said second circuit design by use of direct timing driven placement processes~~

wherein one of b1) and b2) is performed during a pass including c), d), e), and f), wherein b1) is performed during a

first pass, and wherein b2) is performed during any subsequent pass.

13. (Currently Amended) The method of Claim 12 wherein ~~said~~ b1) comprises:

~~b1)~~ placing cells ~~of said first circuit design~~ to minimize total weighted length of wiring interconnecting said cells~~, wherein said b1) placing produces said first placement~~.

14. (Currently Amended) The method of Claim 12 wherein said c) comprises:

c1) estimating ~~congestion for wiring~~ routability to connect said cells~~, wherein said first placement is further a first layout~~.

15. (Currently Amended) The method of Claim 12 ~~further comprising repeating said c), e) and f)~~ wherein at least 4 subsequent passes are performed.

16. (Currently Amended) The method of Claim 12 ~~further comprising repeating said c), d), e) and f)~~ wherein e) comprises:

e1) adding at least one additional cell to minimize signal timing, and

f) comprises:

f1) legalizing any additional cells added during e).

17. (Currently Amended) The method of Claim 12 wherein ~~said d~~ e) comprises:

~~d~~ e1) ~~modifying said first circuit design to achieve minimum~~ minimizing required signal timing within said ~~first~~

layout~~, wherein said di) modifying produces said second circuit design containing second cells~~.

18. (Currently Amended) The method of Claim ~~12~~ 17 wherein ~~said d~~ e1) comprises at least one of:

~~di) modifying said first circuit design to enlarge cell area allocations within congested regions of said first layout, wherein said di) modifying produces said second circuit design containing second cells~~ changing a current-handling capacity of a circuit element and adding a buffer.

19. (Currently Amended) A system comprising:

a processor coupled to a bus;

a memory coupled to said bus and wherein said memory contains instructions that when executed implement a method for placing circuit elements on an integrated circuit, said method comprising the steps of:

a) placing cells of a ~~first~~ circuit design without regard to circuit timing~~, wherein said placing produces a first placement~~; ~~and~~

b) providing routing information associated with said cells;

c) performing a detailed placement of said cells using said routing information;

~~b~~ d) placing said cells by use of direct timing driven placement processes~~, wherein said first placement is an input into said b) placing~~; and

e) repeating b) and c) after d) to optimize placement of said cells.

20. (Currently Amended) A system as described in Claim 19 wherein ~~said~~ a) comprises:

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al) ~~placing cells of a first circuit design to minimize~~ minimizing total weighted length of wiring interconnecting said cells~~, wherein said al) placing produces said first placement~~.